(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 May 2005 (06.05.2005)

PCT

(10) International Publication Number
WO 2005/040961 A2

(51) International Patent Classification[7]: G06F

(21) International Application Number:
PCT/US2004/013483

(22) International Filing Date: 30 April 2004 (30.04.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/511,535 15 October 2003 (15.10.2003) US

(71) Applicant *(for all designated States except US)*: **PDF SOLUTIONS, INC.** [US/US]; 333 West San Carlos Street, Suite 700, San Jose, CA 95110 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **HESS, Christopher** [US/US]; 320 South Overlook Drive, San Ramon, CA 94583 (US). **GOLDMAN, David** [US/US]; 1290 S. Monte Cristo Way, Las Vegas, NV 89117-1411 (US).

(74) Agent: **KOFFS, Steven, E.**; Duane Morris LLP, One Liberty Place, Philadelphia, PA 19103-7396 (US).

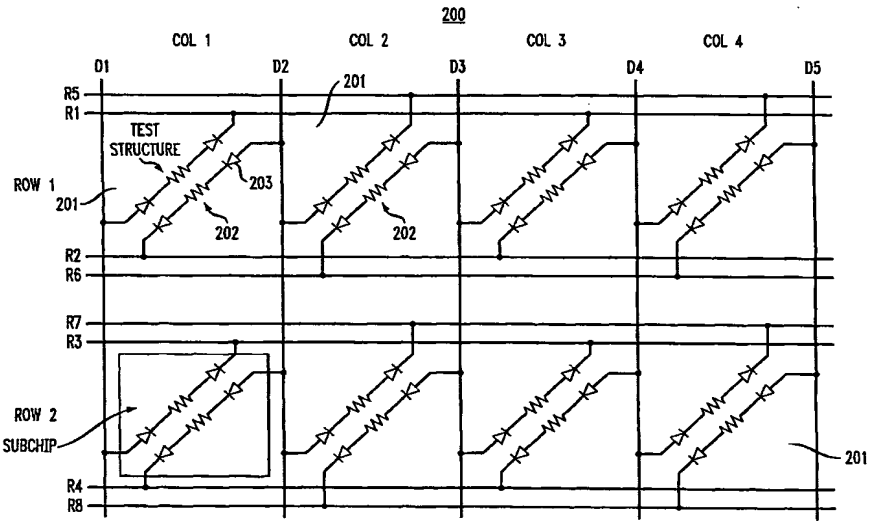
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** METHOD AND CONFIGURATION FOR CONNECTING TEST STRUCTURES OR LINE ARRAYS FOR MONITORING INTEGRATED CIRCUIT MANUFACTURING



(57) **Abstract:** A test chip comprises at least one level having an array of regions. Each region is capable of including at least one test structure. At least some of the regions include respective test structures. The level has a plurality of driver lines that provide input signals to the test structures. The level has a plurality of receiver lines that receive output signals from the test structures. The level has a plurality of devices for controlling current flow. Each test structure is connected to at least one of the driver lines with a first one of the devices in between. Each test structure is connected to at least one of the receiver lines with a second one of the devices in between, so that each of the test structures can be individually addressed for testing using the driver lines and receiver lines.

WO 2005/040961 A2